a non-volatile memory formed in a memory cell region of said semiconductor substrate;

a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode;

a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and

a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode;

said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness,

said first through third gate electrodes having a substantially identical height, wherein the first, second, and third gate electrode each comprise two silicon layers stacked one upon the other.

17. (Amended) A semiconductor integrated circuit as claimed in claim 16, wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first silicon film, said second gate electrode has a structure in which said second silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked.